

**Dual N-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(ON) \max}$	$I_D \max$ $T_A = +25^\circ C$
20V	11.5m $\Omega$ @ $V_{GS} = 4.5V$	10 A
	14m $\Omega$ @ $V_{GS} = 2.5V$	9 A

**Description**

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

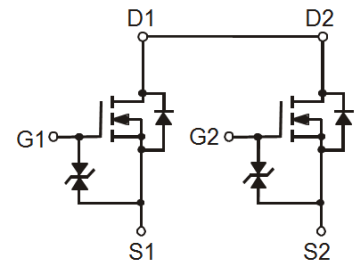
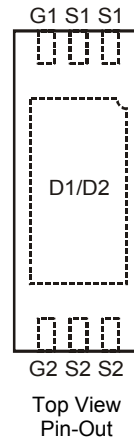
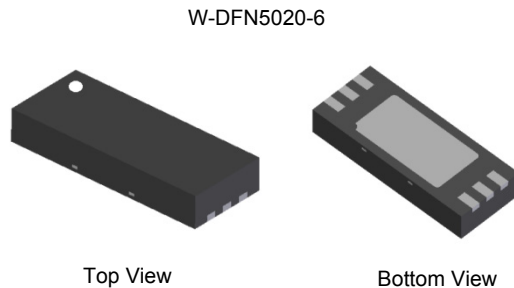
- General Purpose Interfacing Switch
- Power Management Functions

**Features and Benefits**

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected**
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: W-DFN5020-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Weight: 0.03 grams (approximate)



**Ordering Information (Note 4)**

Part Number	Case	Packaging
DMN2013UFX-7	W-DFN5020-6	3000 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



FX = Product Type Marking Code  
 YM = Date Code Marking  
 Y = Year (ex: X = 2010)  
 M = Month (ex: 9 = September)

Date Code Key

Year	2010	2011	2012	2013	2014	2015	2016
Code	X	Y	Z	A	B	C	D

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DSS}$	20	V
Gate-Source Voltage			$V_{GSS}$	$\pm 8$	V
Continuous Drain Current (Note 5) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$	10 8	A
Continuous Drain Current (Note 5) $V_{GS} = 2.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$	9 7	A
Pulsed Drain Current (Note 7)			$I_{DM}$	80	A

**Thermal Characteristics**

Characteristic	Symbol	Max	Unit
Power Dissipation (Note 5)	$P_D$	0.78	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$ (Note 5)	$R_{\theta JA}$	163	$^\circ\text{C/W}$
Power Dissipation (Note 6)	$P_D$	2.14	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$ (Note 6)	$R_{\theta JA}$	59	$^\circ\text{C/W}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
<b>OFF CHARACTERISTICS (Note 8)</b>							
Drain-Source Breakdown Voltage	$BV_{DSS}$	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$	
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$	
<b>ON CHARACTERISTICS (Note 8)</b>							
Gate Threshold Voltage	$V_{GS(th)}$	0.5	—	1.1	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	8.4	11.5	m $\Omega$	$V_{GS} = 4.5\text{V}, I_D = 8.5\text{A}$	
			8.5	12.0			$V_{GS} = 4.0\text{V}, I_D = 8.5\text{A}$
			8.6	12.5			$V_{GS} = 3.5\text{V}, I_D = 8.5\text{A}$
			9.0	13.5			$V_{GS} = 3.1\text{V}, I_D = 8\text{A}$
			9.6	14.0			$V_{GS} = 2.5\text{V}, I_D = 8\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	18.2	—	S	$V_{DS} = 5\text{V}, I_D = 4\text{A}$	
Diode Forward Voltage	$V_{SD}$	—	—	1.2	V	$V_{GS} = 0\text{V}, I_S = 8.5\text{A}$	
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>							
Input Capacitance	$C_{iss}$	—	2607	—	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	
Output Capacitance	$C_{oss}$	—	255	—	pF		
Reverse Transfer Capacitance	$C_{rss}$	—	236	—	pF		
Gate Resistance	$R_g$	—	1.2	—	$\Omega$	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	
Total Gate Charge ( $V_{GS} = 4.5\text{V}$ )	$Q_g$	—	32.4	—	nC	$V_{DS} = 10\text{V}, I_D = 8.5\text{A}$	
Total Gate Charge ( $V_{GS} = 8\text{V}$ )	$Q_g$	—	57.4	—	nC		
Gate-Source Charge	$Q_{gs}$	—	3.5	—	nC		
Gate-Drain Charge	$Q_{gd}$	—	4.0	—	nC		
Turn-On Delay Time	$t_{D(on)}$	—	8.6	—	ns		
Turn-On Rise Time	$t_r$	—	20.3	—	ns	$V_{DS} = 10\text{V}, I_D = 8.5\text{A}$ $V_{GS} = 4.5\text{V}, R_G = 1.8\Omega$	
Turn-Off Delay Time	$t_{D(off)}$	—	42.5	—	ns		
Turn-Off Fall Time	$t_f$	—	13.7	—	ns		

- Notes:
- Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate
  - Repetitive rating, pulse width limited by junction temperature.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

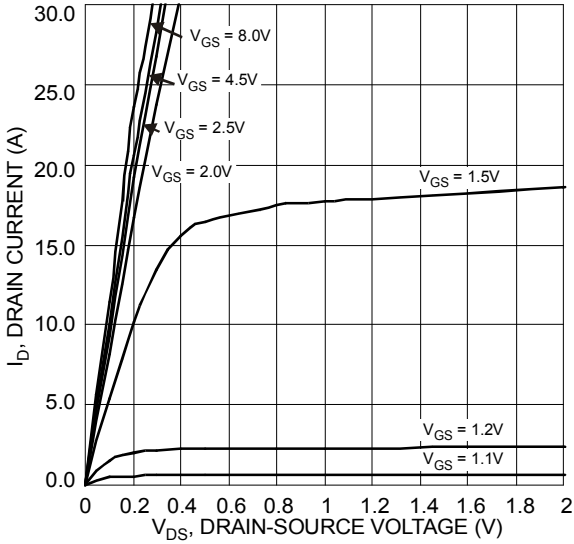


Figure 1 Typical Output Characteristic

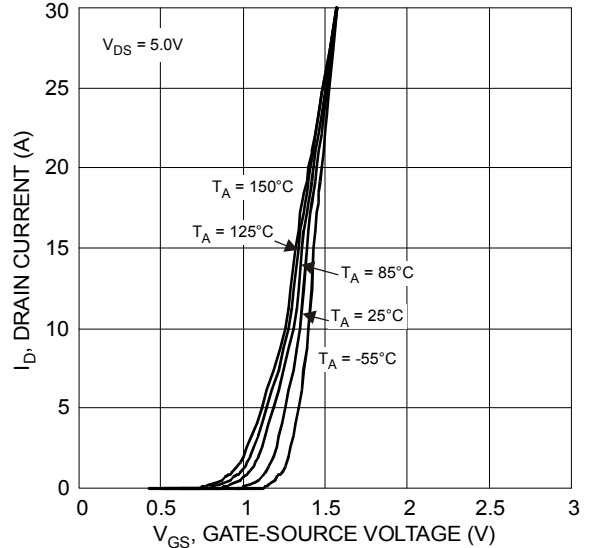


Figure 2 Typical Transfer Characteristics

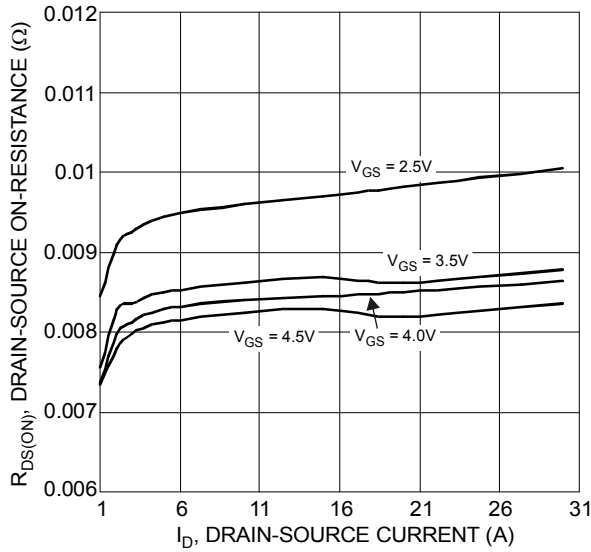


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

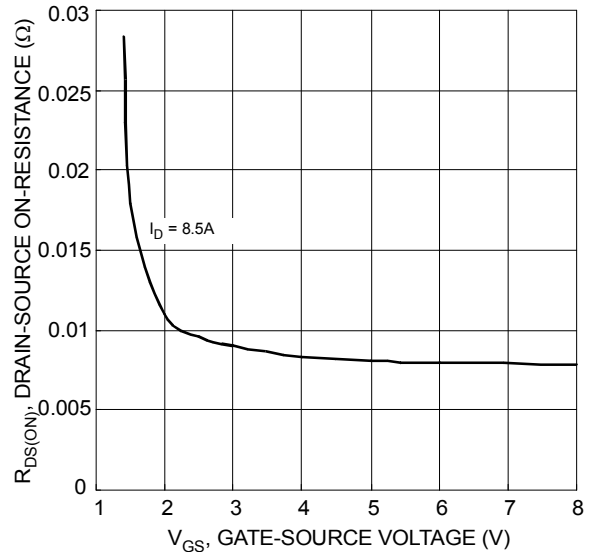


Figure 4 Typical Transfer Characteristic

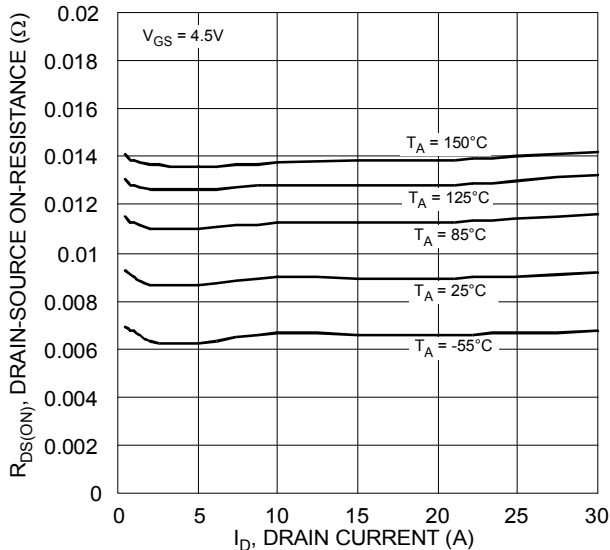


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

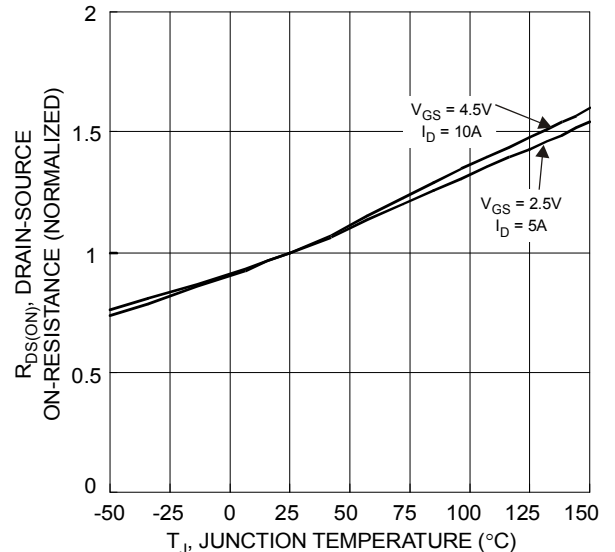


Figure 6 On-Resistance Variation with Temperature

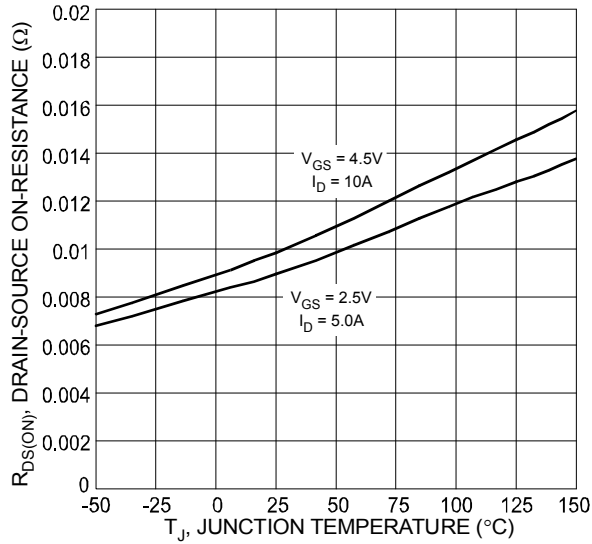


Figure 7 On-Resistance Variation with Temperature

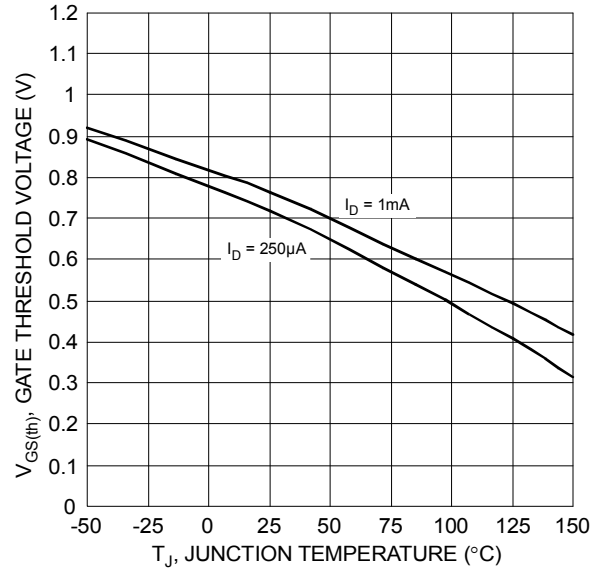


Figure 8 Gate Threshold Variation vs. Ambient Temperature

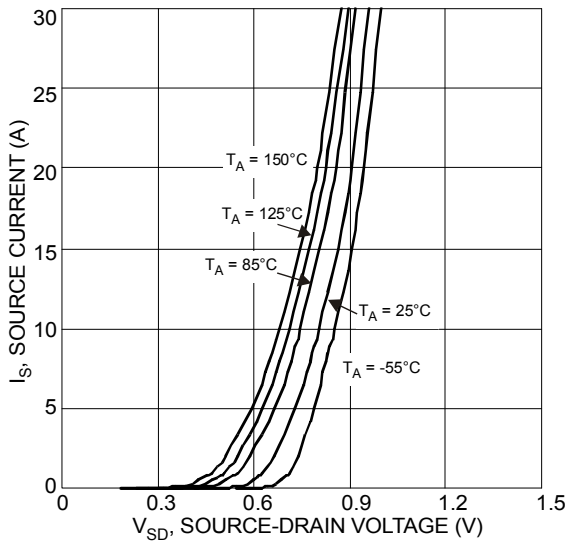


Figure 9 Diode Forward Voltage vs. Current

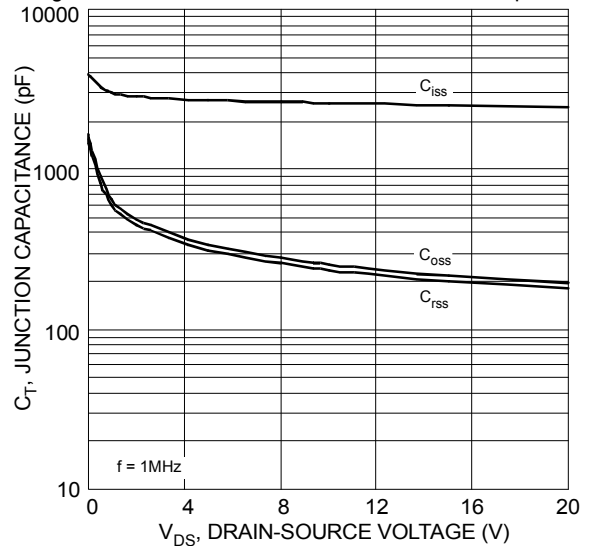


Figure 10 Typical Junction Capacitance

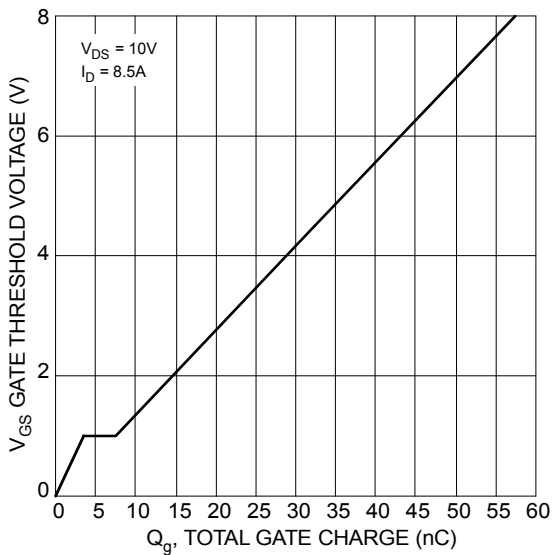
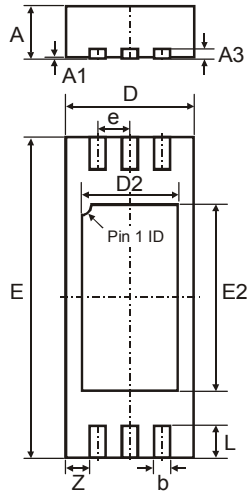


Figure 11 Gate Charge

## Package Outline Dimensions

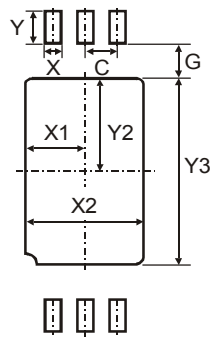
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



W-DFN5020-6			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	1.90	2.10	2.00
D2	1.40	1.60	1.50
e	-	-	0.50
E	4.90	5.10	5.00
E2	2.80	3.00	2.90
L	0.35	0.65	0.50
Z	-	-	0.375
All Dimensions in mm			

## Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.50
G	0.35
X	0.35
X1	0.90
X2	1.80
Y	0.70
Y2	1.60
Y3	3.20

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